ANALYSIS AND MINIMIZATION OF LOW POWER VLSI DESIGN BY USING DYNAMIC PHASE FREQUENCY DETECTOR IN ADPLL

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ABSTRACT

A dynamic phase frequency detector has been used which mainly concentrates on reducing the power consumption, and has the ability of fast locking and reducing the delay moments. A low power All Digital Phase Locked Loop (ADPLL) have become more attractive because they yield better testability, programmability, stability, and portability over different processes and the ADPLL has better noise immunity. The goal of the Time-to-Digital Converter TDC is to measure the time difference between the rising edges of the signals. A phase prediction algorithm via the assistance of the DTC reduces required TDC range thus saving substantial power. The complete ADPLL system improves the performance of the locking ability and the system DTC linearity. The design is implemented using DPFD technique was more suitable for high speed phase frequency detector. The proposed system of dynamic phase frequency detector has been fabricated and the corresponding power consumed is 20 µW.

Keywords--All Digital Phase Locked Loop (ADPLL), Time to Digital Converter (TDC), Dynamic Phase Frequency Detector (DPFD)

I. INTRODUCTION

A Time-to-digital converter (TDC) is similar to an analog-to digital converter (ADC), except that, instead of quantizing voltage or current, the TDC quantizes time intervals between two rising edges. It is originally developed for nuclear experiments to locate single-shot events , the TDC is now being used in many applications such as laser range finders, space science instruments, physical instruments, phase meters, high energy particle detectors, and digital storage oscilloscopes and measurement devices. Recently, it has been employed to measure phase in all-digital phase-locked loops (PLLs).

Precise measurements of time interval are performed with the use of various methods in both the analog and digital domains. The digital methods become dominant due to ease of implementation in integrated circuits, shorter conversion time, and higher immunity to external disturbances. First, the physical quantity is converted to a time signal and then digitized by a time-to digital converter (TDC) to get the corresponding digital output.

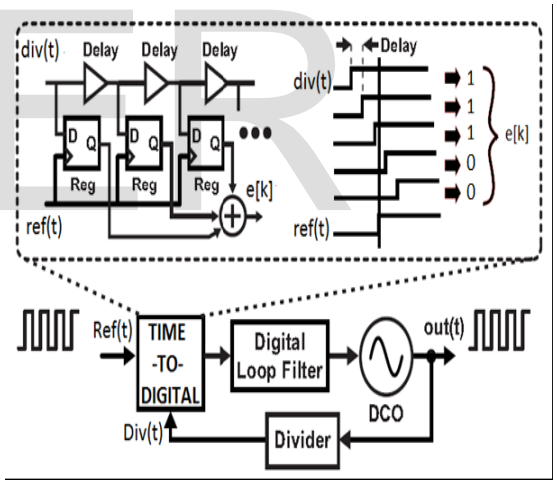

Fig.1. TDC in All-Digital Phase-Locked Loop

An ADPLL with a novel fine-tuning delay cell is presented. It can reduce both cost and design time for building a high-resolution cell-based DCO. The proposed frequency tracking algorithm, which uses an adaptive search step, can achieve fast lock-in time. We have also further reduced the dead zone effect, developed small and compact layout architecture, improved the total power dissipations and introduced a low power supply which is 1.2 V compared to 1.8 V used at the power consumption.

This paper is organized as follows: Section II describes the Proposed Algorithm, Section III details the implementation of the major circuit blocks, and Section IV reports the most relevant

measurement results. Conclusions are finally drawn in Section V.

II. PROPOSED ALGORITHM

Dynamic CMOS logic circuits and especially domino-logic have been used in high-performance designs due to their faster operating speed and potential saving in power. Several dynamic-logic PFDs were introduced .A pioneer dynamic-logic (domino-logic) PFD is shown in fig.2.

The only way to increase the detection range of the DPFD is to decrease the reset time of the PFD. The reset time of the DPFD is actually given by the sum of the discharge time of pre-charge-node of first stage, the charging time of pre-charge-node of second stage and the discharge time of the output inverter. During the reset operation, the DPFD can be considered as cascade connection of three inverter stages. It consists of transistors U2-U3 (D2-D3), U5-U6 (D5-D6) and U8-U9 (D8-D9). So by proper inverter sizing, the inverter delay is reduced.

The inverter sizing factor 'f' selected is 1.3. This will decrease the reset time and in turn increase the detection range of the DPFD. The next step is the modification of the circuit architecture to reduce the signal path length. This will increase the speed of the PFD. Looking into the circuit diagram given in Fig. 2; it can be observed that the transistor U6 (D6) causes increase in capacitance and resistance in the signal path. This will cause excess delay in the circuit which increases the reset time. By interchanging the transistors U6 and U7 (D6 and D7), the signal path length is reduced because the resistance and capacitance U6 (D6) will not come in the signal path. This will reduce the delay of the circuit and in turn, the reset time. As the final step, pre-charge transistors are included to further increase the detection range of the DPFD.

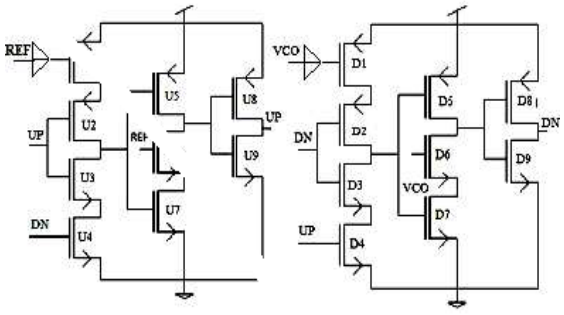

Fig.2.A pioneer domino-logic PFD

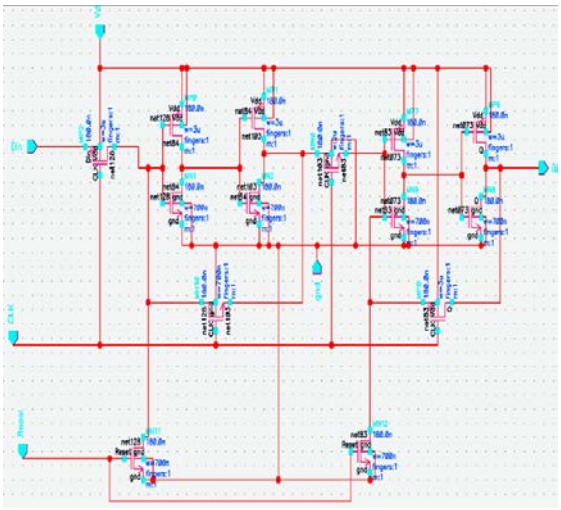

Fig.3.Schematic diagram of Dynamic PFD

In an effort to design a PFD capable of working at gigahertz frequency with minimum dead-zone, minimum phase offset and reduced blind-zone, we have proposed a new domino-logic PFD. Our design goals are accomplished by overcoming the drawbacks existing in previous dynamic PFDs. Circuit integrity is maintained in this design. The new PFD is shown in fig.4. MU2-3 and MD2-3 form two inverter structures in the pre-charge stage that basically prevent the device from fig:4.

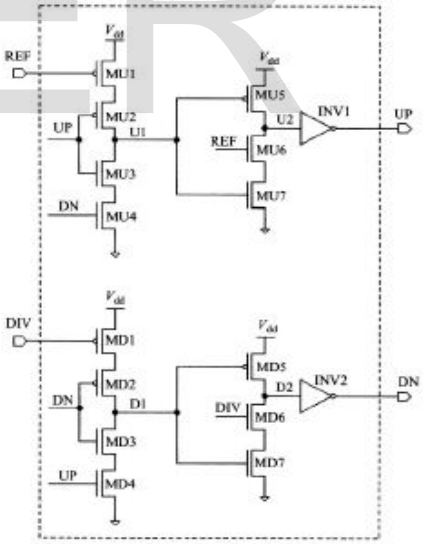

Fig.4.Dynamic PFD

It should become obvious that the circuit will be fully operational with a permutation of MU1 and MU2, MU3 and MU4 (also MD1 and MD2, MD3 and MD4).

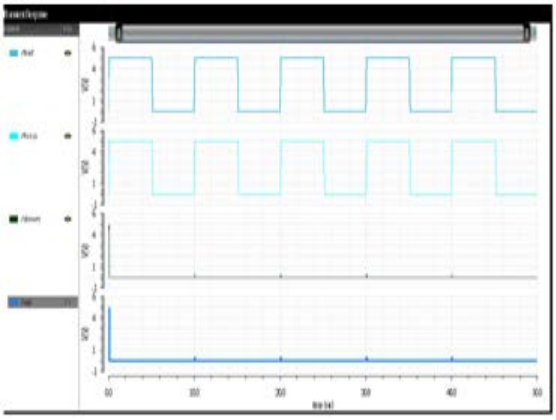

Fig.5.Simulated output, of DPFD when input signals are synchronous.

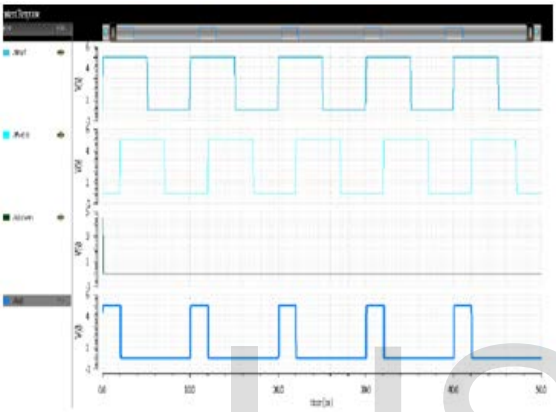

Fig.6.Simulated output, of PFD when clk out is leading

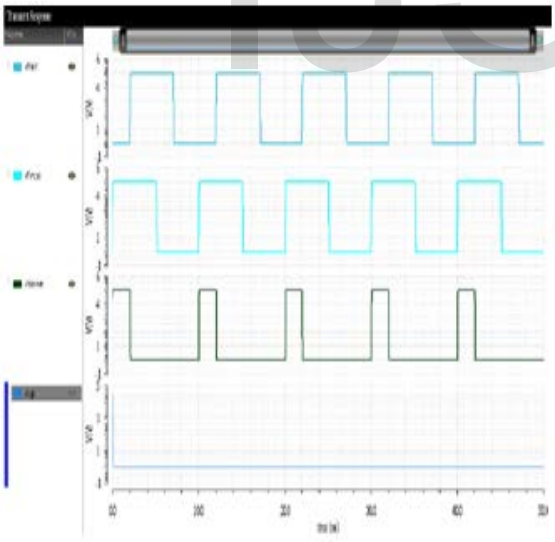

Fig.7.output waveform of DPFD

III. IMPLEMENTATION

The block diagram of proposed ADPLL is shown in Fig.8. Vernier delay line TDC in Fig. 2b requires 25 transistors in an implementation one D flip-flop Fig. 3 requires nine transistors per stage. Hence, the proposed ADPLL transistor count is mainly reduced by the TDC circuit.

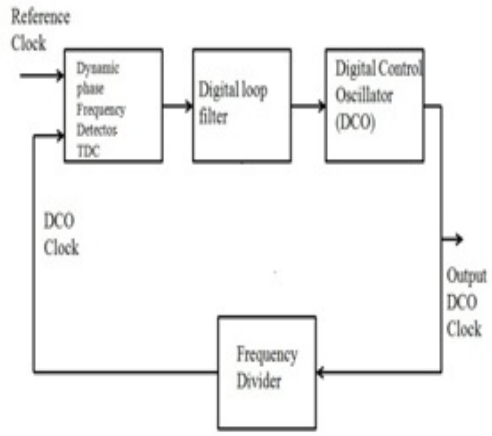

Fig.8.Block diagram of proposed system

A. TIME TO DIGITAL CONVERTER

To allow for implementation margin, instead of 8, 16 dithering elements were implemented in the first on-chip FREF buffer. The dithering range was specified to cover at least two worst case $\Delta tres$ steps of 30ps. A schematic of the physical TDC circuit implementation is shown in Figure 9. (a) in which the fine dithering digital bits F0-F15 modulate the bias current of the slicer, which results in a minimum dithering step of 4 ps across process

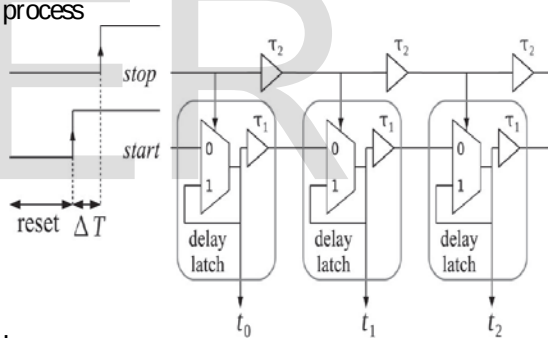

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Fig.9. Illustration of the proposed delay latch chain TDC

B. Delay Latch Chain

A complete conversion cycle for the proposed architecture in Fig. 9 consists of the following steps,

1) The TDC is prepared for conversion in the reset phase, where the start and stop inputs are low. All delay latches are now transparent.

2) At the next rising edge of the start input, a pulse propagates through the delay latch chain gradually increasing the thermometer code at the t_x outputs.

3) At the next rising edge of the stop input, a second pulse propagates through the delay line continuously setting the delay latches in hold state.

4) When the stop pulse catches up with the start pulse, the

Nth delay latch is non transparent, hereby stopping the propagation of the start pulse.

5) The thermometer code, i.e., t_x, at the output of the delay latches is now linearly dependent on the time difference, i.e., ΔT, between the two inputs.

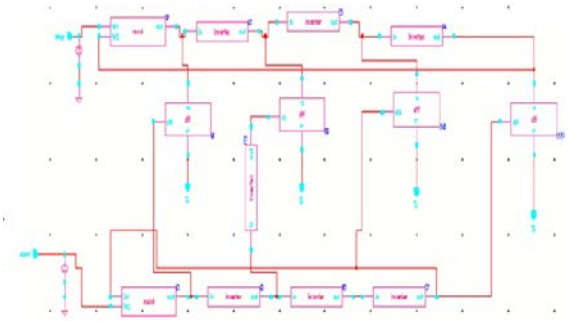

Fig.10.Schematic design of TDC.

C. Digital Loop Filter

The schematic diagram of digital loop filter shown in fig.11 Since the conventional phase/frequency detector and charge pump, which encode the phase error by the width of the train of pulses at FREF rate, are replaced by the TDC, the phase-domain operation does not fundamentally generate any reference spurs thus allowing for the digital loop filter to be set at an optimal performance point between the reference phase noise and the oscillator phase noise. Consequently, the ADPLL for Bluetooth is merely designed to provide only the first or second order filtering, in contrast to the third-order filtering for the traditional PLLs. The cellular systems, however, require better filtering, and sharply attenuate phase noise at the protected 400 kHz frequency offset. Such sharp filtering would not be possible in a controlled manner with the traditional PLLs.

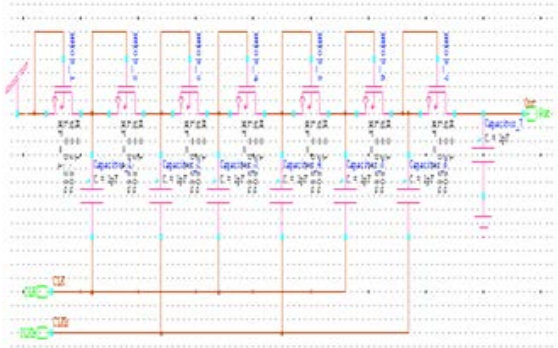

Fig.11.Schematic design of digital loop filter

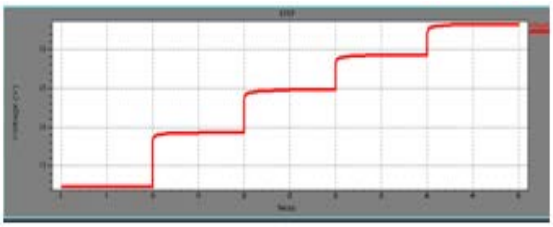

Fig.12.Simulation result of digital loop filter.

D. Digital Controlled Oscillator (DCO)

The DCO is a three-staged ring oscillator that consists of a couple of normal delay cells (Type-1) and one delay cell with a phase-shifting function (Type-2). For a resettable design, we employed the last delay cell of type-2. When *rst* is asserted to 0, the last cell is transformed from an inverting buffer to a non inverting buffer. Since the remaining first two delay cells are initialized with the same value, i.e., 1 at and 0 at and the total phase shift over the DCO becomes 360 at this condition, the DCO stops oscillating and keeps this status. Once *rst* returns to 1, the DCO resumes oscillating from this reset status. In this design, voltage swing of each delay cell is determined as by the replica bias circuit. Every delay cell has a differential structure for an immunity to supply noises. The digital capacitance tuning is normally realized by adding or removing some unit-sized varactors, so the smallest frequency step size, corresponding to the minimum capacitance step size, is usually limited by the smallest varactor size for a given technology. In this work, a capacitance tuning scheme with incrementally-sized varactors and matched varactor banks is employed. It can achieve both high frequency resolution (approximately 6kHz) and large linear frequency tuning range with small differential nonlinearity.

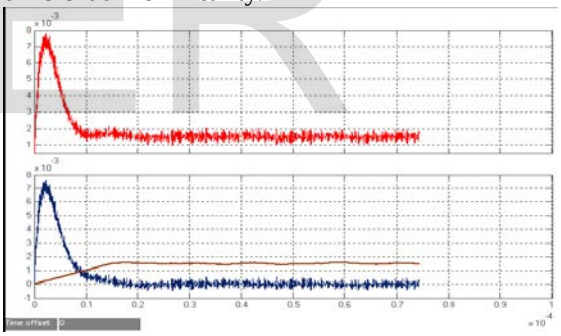

Fig.13.Output waveform of digital controlled oscillator

E. Frequency Divider

The frequency divider Schematic design is shown in Fig. 14. The output of the DCO needs to be divided to match the reference frequency. The implementation contains a divide by four frequency divider, enabling the PLL to have a multiplication factor of four. The divider is implemented by using two series D Flip-flops. The DCO clock is input into both flip-flops and the non-inverted output of the second flip-flop is the DCO clock divided by four lock occurred. The PFD continues to analyze the divided DCO clock signal with the reference clock signal for any variations. A frequency or phase variation will cause the PFD to become activated and the synchronization of two clocks will be achieved again. Figure 14 shows the

schematic of the PLL system, a better resolution image is attached.

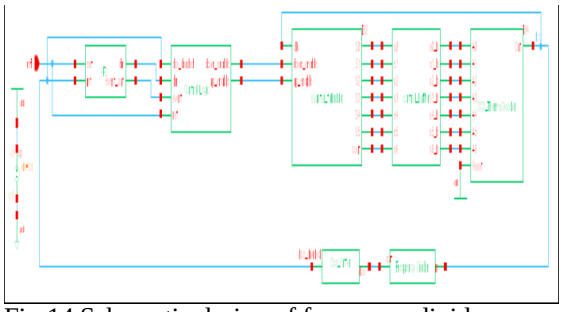

Fig.14.Schematic design of frequency divider

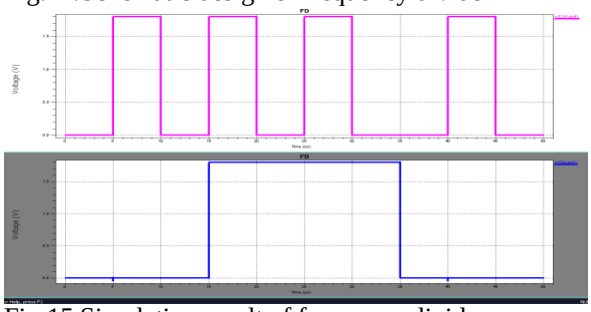

Fig.15.Simulation result of frequency divider.

IV. EXPERIMENTAL RESULTS

The proposed algorithm with over all implementation in ADPLL with the dynamic phase frequency detector and it consumes the power of 76.8 µW from a 1.2 V supply. The proposed system is to design a low power ADPLL using a dynamic phase frequency detector consumes the power of 20µW ADPLL was implemented in a standard IBM 13 CMOS process technology.

Table 1
Power comparison

Type	Power µw
PFD	6.77 mW
DPFD	78.6 µW

V. CONCLUSION

In this work, ADPLL architecture dynamic phase frequency detector maximum power consumption is 78.6µW from a 1.2 V supply. On comparing the various parameters of phase frequency detector architecture in ADPLL provides the better solution of fast locking, high noise immunity, consumes low power, and does not need voters and reduces area overhead significantly.

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